

To our customers,

---

## Old Company Name in Catalogs and Other Documents

---

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

## Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
  - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
  - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
  - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

To all our customers

---

## **Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.**

---

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

## Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

---

# HN58X24128FPIAG HN58X24256FPIAG

Two-wire serial interface  
128k EEPROM (16-kword × 8-bit)  
256k EEPROM (32-kword × 8-bit)



ADE-203-1266A (Z)  
Rev. 1.0  
Apr. 20, 2001

---

## Description

HN58X24xxxFPIAG series are two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). They realize high speed, low power consumption and a high level of reliability by employing advanced MNOS memory technology and CMOS process and low voltage circuitry technology. They also have a 64-byte page programming function to make their write operation faster.

## Features

- Single supply: 1.8 V to 5.5 V
- Two-wire serial interface (I<sup>2</sup>C™ serial bus\*<sup>1</sup>)
- Clock frequency: 400 kHz
- Power dissipation:
  - Standby: 3 μA (max)
  - Active (Read): 1 mA (max)
  - Active (Write): 5 mA (max)
- Automatic page write: 64-byte/page
- Write cycle time: 10 ms (2.7 V to 5.5 V)/15 ms (1.8 V to 2.7 V)
- Endurance: 10<sup>5</sup> Cycles (Page write mode)
- Data retention: 10 Years

# HN58X24128FPIAG/HN58X24256FPIAG

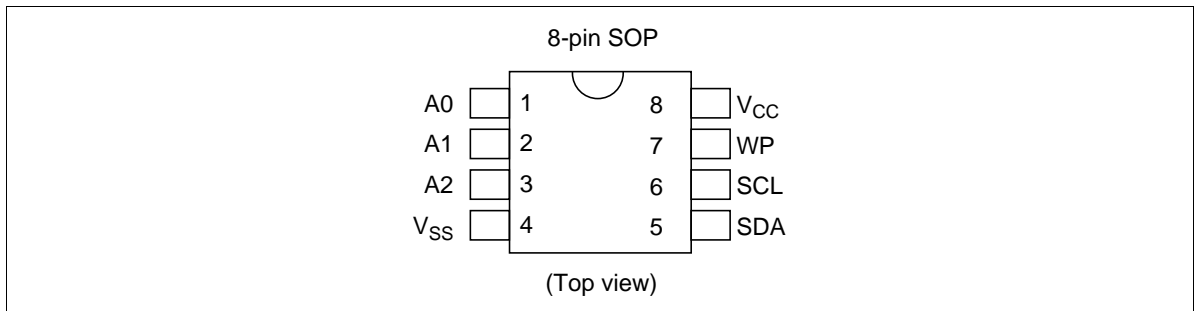
- Small size packages: SOP-8pin
- Shipping tape and reel: 2,500 IC/reel
- Temperature range: -40 to +85°C

Note: 1. I<sup>2</sup>C is a trademark of Philips Corporation.

## Ordering Information

Type No.	Internal organization	Operating voltage	Frequency	Package
HN58X24128FPIAG	128k bit (16384 × 8-bit)	1.8 V to 5.5 V	400 kHz	150 mil 8-pin plastic SOP (FP-8DB)
HN58X24256FPIAG	256k bit (32768 × 8-bit)			

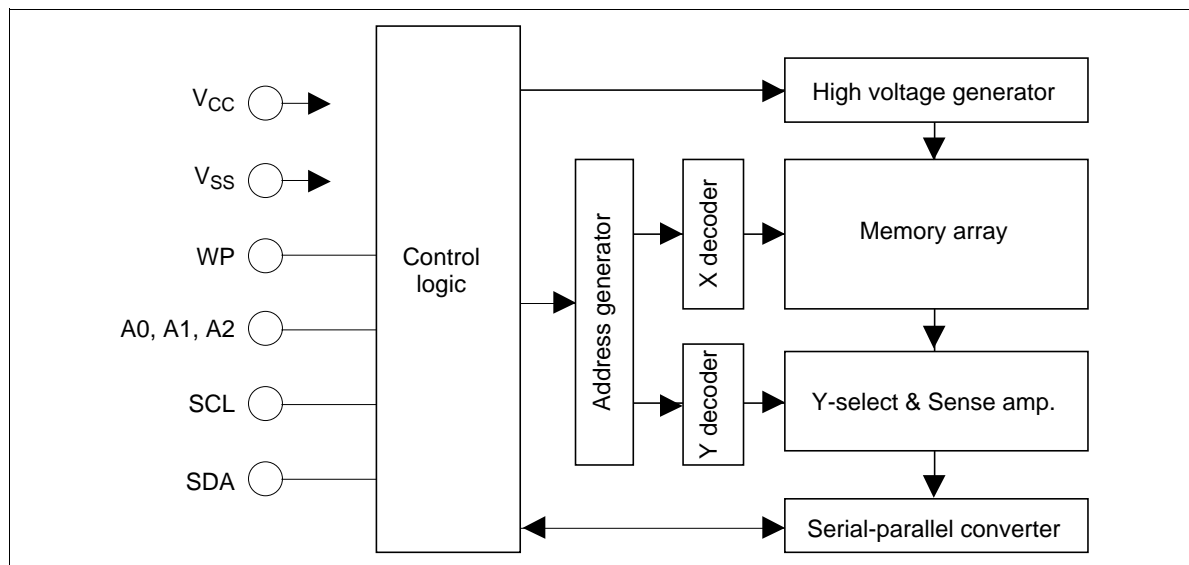
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A2	Device address
SCL	Serial clock input
SDA	Serial data input/output
WP	Write protect
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

## Block Diagram



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.6 to +7.0	V
Input voltage relative to $V_{SS}$	$V_{in}$	-0.5*2 to +7.0*3	V
Operating temperature range*1	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to +125	°C

Notes: 1. Including electrical characteristics and data retention.

2.  $V_{in}$  (min): -3.0 V for pulse width  $\leq$  50 ns.

3. Should not exceed  $V_{CC} + 1.0$  V.

## DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	1.8	—	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	$V_{CC} \times 0.7$	—	$V_{CC} + 1.0$	V
Input low voltage	$V_{IL}$	-0.3*1	—	$V_{CC} \times 0.3$	V
Operating temperature	$T_{opr}$	-40	—	85	°C

Notes: 1.  $V_{IL}$  (min): -1.0 V for pulse width  $\leq$  50 ns.

# HN58X24128FPIAG/HN58X24256FPIAG

## DC Characteristics (Ta = -40 to +85°C, V<sub>CC</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	2.0	μA	V <sub>CC</sub> = 5.5 V, Vin = 0 to 5.5 V
Output leakage current	I <sub>LO</sub>	—	—	2.0	μA	V <sub>CC</sub> = 5.5 V, Vout = 0 to 5.5 V
Standby V <sub>CC</sub> current	I <sub>SB</sub>	—	1.0	3.0	μA	Vin = V <sub>SS</sub> or V <sub>CC</sub>
Read V <sub>CC</sub> current	I <sub>CC1</sub>	—	—	1.0	mA	V <sub>CC</sub> = 5.5 V, Read at 400 kHz
Write V <sub>CC</sub> current	I <sub>CC2</sub>	—	—	5.0	mA	V <sub>CC</sub> = 5.5 V, Write at 400 kHz
Output low voltage	V <sub>OL2</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 1.6 mA V <sub>CC</sub> = 2.7 to 4.5 V, I <sub>OL</sub> = 0.8 mA V <sub>CC</sub> = 1.8 to 2.7 V, I <sub>OL</sub> = 0.4 mA
	V <sub>OL1</sub>	—	—	0.2	V	V <sub>CC</sub> = 1.8 to 2.7 V, I <sub>OL</sub> = 0.2 mA

## Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance (A0 to A2, SCL, WP)	C <sub>in</sub> *1	—	—	6.0	pF	Vin = 0 V
Output capacitance (SDA)	C <sub>I/O</sub> *1	—	—	6.0	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.



**AC Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.8$  to  $5.5$  V)

**Test Conditions**

- Input pules levels:
  - $V_{IL} = 0.2 \times V_{CC}$
  - $V_{IH} = 0.8 \times V_{CC}$
- Input rise and fall time:  $\leq 20$  ns
- Input and output timing reference levels:  $0.5 \times V_{CC}$
- Output load: TTL Gate + 100 pF

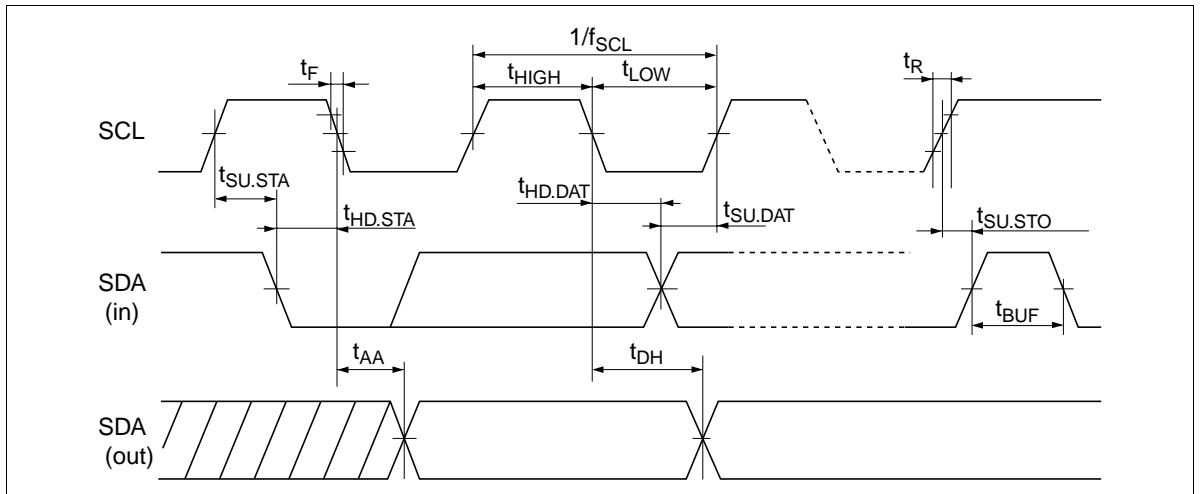
Parameter	Symbol	Min	Typ	Max	Unit	Notes	
Clock frequency	$f_{SCL}$	—	—	400	kHz		
Clock pulse width low	$t_{LOW}$	1200	—	—	ns		
Clock pulse width high	$t_{HIGH}$	600	—	—	ns		
Noise suppression time	$t_i$	—	—	50	ns	1	
Access time	$t_{AA}$	100	—	900	ns		
Bus free time for next mode	$t_{BUF}$	1200	—	—	ns		
Start hold time	$t_{HD.STA}$	600	—	—	ns		
Start setup time	$t_{SU.STA}$	600	—	—	ns		
Data in hold time	$t_{HD.DAT}$	0	—	—	ns		
Data in setup time	$t_{SU.DAT}$	100	—	—	ns		
Input rise time	$t_R$	—	—	300	ns	1	
Input fall time	$t_F$	—	—	300	ns	1	
Stop setup time	$t_{SU.STO}$	600	—	—	ns		
Data out hold time	$t_{DH}$	50	—	—	ns		
Write cycle time	$V_{CC} = 2.7$ V to $5.5$ V	$t_{WC}$	—	—	10	ms	2
	$V_{CC} = 1.8$ V to $2.7$ V	$t_{WC}$	—	—	15	ms	2

Notes: 1. This parameter is sampled and not 100% tested.

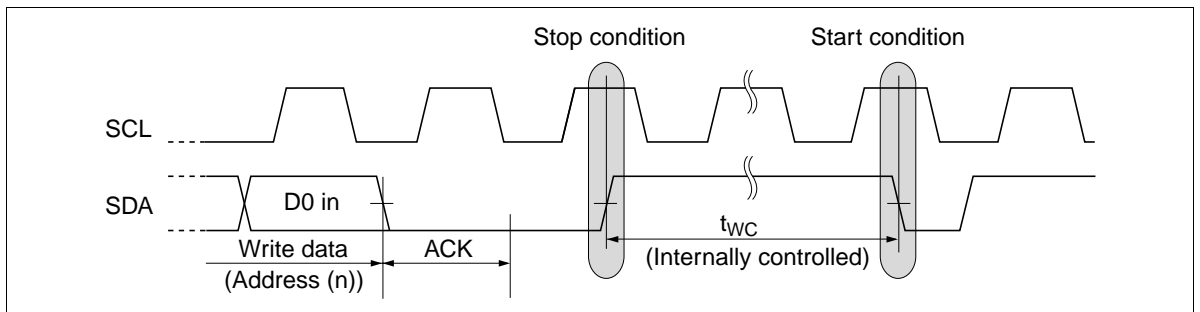
2.  $t_{WC}$  is the time from a stop condition to the end of internally controlled write cycle.

## Timing Waveforms

### Bus Timing



### Write Cycle Timing



## Pin Function

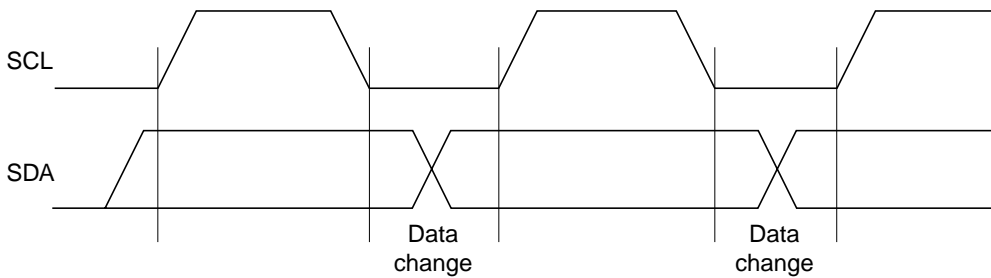
### Serial Clock (SCL)

The SCL pin is used to control serial input/output data timing. The SCL input is used to positive edge clock data into EEPROM device and negative edge clock data out of each device. Maximum clock rate is 400 kHz.

### Serial Input/Output Data (SDA)

The SDA pin is bidirectional for serial data transfer. The SDA pin needs to be pulled up by resistor as that pin is open-drain driven structure. Use proper resistor value for your system by considering  $V_{OL}$ ,  $I_{OL}$  and the SDA pin capacitance. Except for a start condition and a stop condition which will be discussed later, the SDA transition needs to be completed during SCL low period.

### Data Validity (SDA data change timing waveform)



Note: High-to-low and low-to-high change of SDA should be done during SCL low periods.

# HN58X24128FPIAG/HN58X24256FPIAG

## Device Address (A0, A1, A2)

Eight devices can be wired for one common data bus line as maximum. Device address pins are used to distinguish each device and device address pins should be connected to  $V_{CC}$  or  $V_{SS}$ . When device address code provided from SDA pin matches corresponding hard-wired device address pins A0 to A2, that one device can be activated.

## Pin Connections for A0 to A2

Memory size	Max connect number	Pin connection			Note
		A2	A1	A0	
128k bit	8	$V_{CC}/V_{SS}^{*1}$	$V_{CC}/V_{SS}$	$V_{CC}/V_{SS}$	
256k bit	8	$V_{CC}/V_{SS}$	$V_{CC}/V_{SS}$	$V_{CC}/V_{SS}$	

Note: 1. " $V_{CC}/V_{SS}$ " means that device address pin should be connected to  $V_{CC}$  or  $V_{SS}$ .

## Write Protect (WP)

When the Write Protect pin (WP) is high, the write protection feature is enabled and operates as shown in the following table. When the WP is low, write operation for all memory arrays are allowed. The read operation is always activated irrespective of the WP pin status. WP should be fixed high or low during operations since WP does not provide a latch function.

## Write Protect Area

WP pin status	Write protect area	
	128k bit	256k bit
$V_{IH}$	Upper 1/8 (16k bit)	Upper 1/8 (32k bit)
$V_{IL}$	Normal read/write operation	

## Functional Description

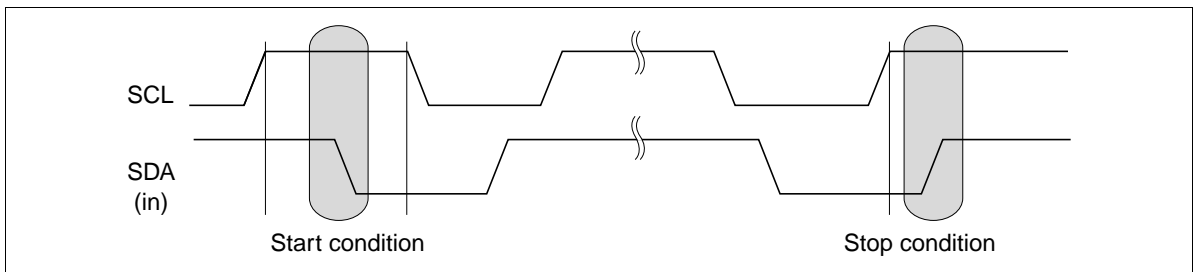
### Start Condition

A high-to-low transition of the SDA with the SCL high is needed in order to start read, write operation. (See start condition and stop condition)

### Stop Condition

A low-to-high transition of the SDA with the SCL high is a stop condition. The stand-by operation starts after a read sequence by a stop condition. In the case of write operation, a stop condition terminates the write data inputs and place the device in a internally-timed write cycle to the memories. After the internally-timed write cycle which is specified as  $t_{WC}$ , the device enters a standby mode. (See write cycle timing)

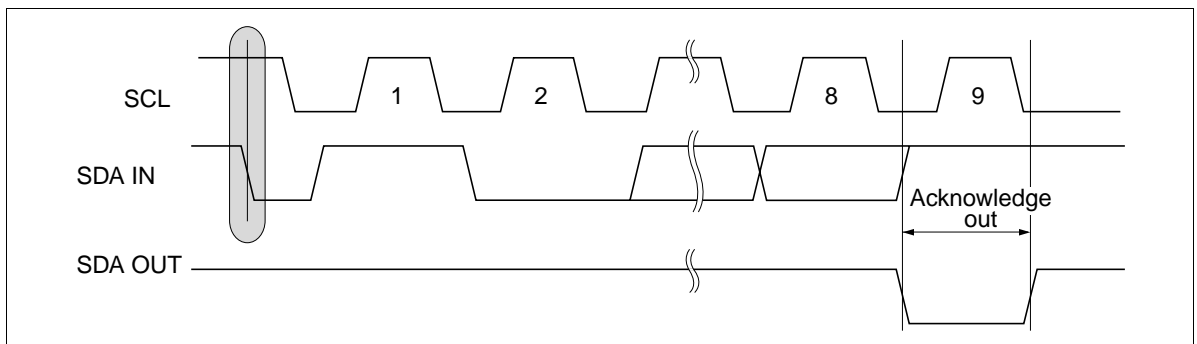
### Start Condition and Stop Condition



## Acknowledge

All addresses and data words are serially transmitted to and from in 8-bit words. The receiver sends a zero to acknowledge that it has received each word. This happens during ninth clock cycle. The transmitter keeps bus open to receive acknowledgment from the receiver at the ninth clock. In the write operation, EEPROM sends a zero to acknowledge after receiving every 8-bit words. In the read operation, EEPROM sends a zero to acknowledge after receiving the device address word. After sending read data, the EEPROM waits acknowledgment by keeping bus open. If the EEPROM receives zero as an acknowledge, it sends read data of next address. If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, it stops the read operation and enters a stand-by mode. If the EEPROM receives neither acknowledgment "0" nor a stop condition, the EEPROM keeps bus open without sending read data.

## Acknowledge Timing Waveform



## Device Addressing

The EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or a write operation. The device address word consists of 4-bit device code, 3-bit device address code and 1-bit read/write(R/W) code. The most significant 4-bit of the device address word are used to distinguish device type and this EEPROM uses “1010” fixed code. The device address word is followed by the 3-bit device address code in the order of A2, A1, A0. The device address code selects one device out of all devices which are connected to the bus. This means that the device is selected if the inputted 3-bit device address code is equal to the corresponding hard-wired A2-A0 pin status. The eighth bit of the device address word is the read/write(R/W) bit. A write operation is initiated if this bit is low and a read operation is initiated if this bit is high. Upon a compare of the device address word, the EEPROM enters the read or write operation after outputting the zero as an acknowledge. The EEPROM turns to a stand-by state if the device code is not “1010” or device address code doesn’t coincide with status of the correspond hard-wired device address pins A0 to A2.

## Device Address Word

Device address word (8-bit)								
Device code (fixed)				Device address code			R/W code*1	
128k, 256k	1	0	1	0	A2	A1	A0	R/W

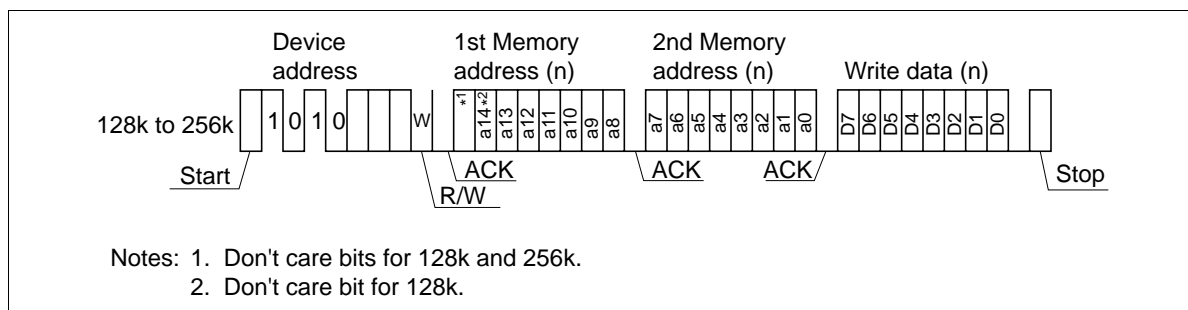
Note: 1. R/W=“1” is read and R/W = “0” is write.

## Write Operations

### Byte Write:

A write operation requires an 8-bit device address word with R/W = "0". Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 128kbit and 256kbit EEPROMs receive 2 sequence 8-bit memory address words. Upon receipt of this memory address, the EEPROM outputs acknowledgment "0" and receives a following 8-bit write data. After receipt of write data, the EEPROM outputs acknowledgment "0". If the EEPROM receives a stop condition, the EEPROM enters an internally-timed write cycle and terminates receipt of SCL, SDA inputs until completion of the write cycle. The EEPROM returns to a standby mode after completion of the write cycle.

### Byte Write Operation

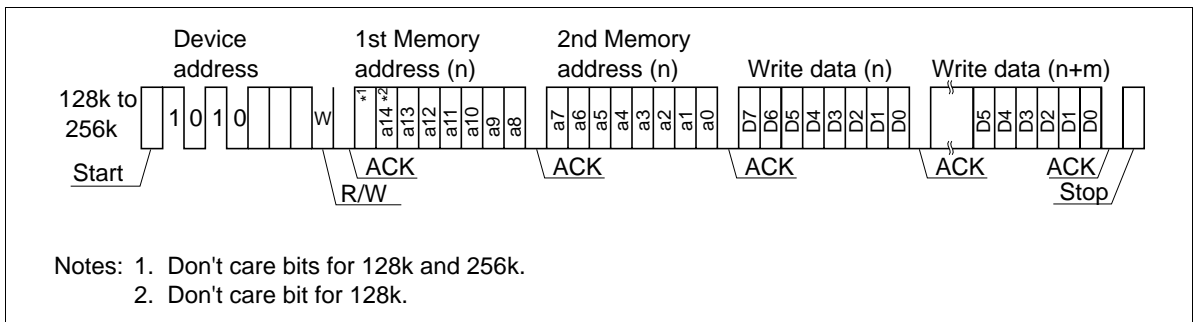




## Page Write:

The EEPROM is capable of the page write operation which allows any number of bytes up to 64 bytes to be written in a single write cycle. The page write is the same sequence as the byte write except for inputting the more write data. The page write is initiated by a start condition, device address word, memory address(n) and write data (Dn) with every ninth bit acknowledgment. The EEPROM enters the page write operation if the EEPROM receives more write data (Dn+1) instead of receiving a stop condition. The a0 to a5 address bits are automatically incremented upon receiving write data (Dn+1). The EEPROM can continue to receive write data up to 64 bytes. If the a0 to a5 address bits reaches the last address of the page, the a0 to a5 address bits will roll over to the first address of the same page and previous write data will be overwritten. Upon receiving a stop condition, the EEPROM stops receiving write data and enters internally-timed write cycle.

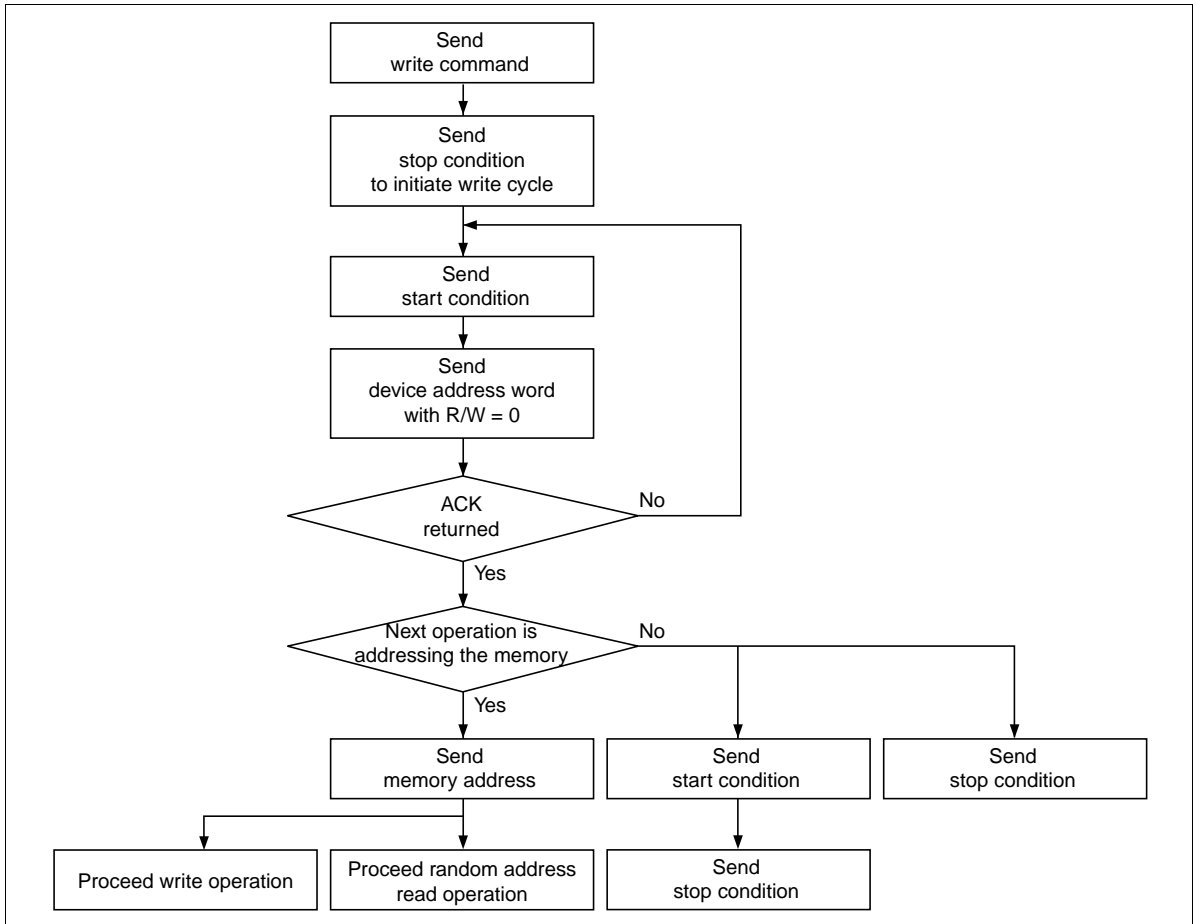
## Page Write Operation



## Acknowledge Polling:

Acknowledge polling feature is used to show if the EEPROM is in a internally-timed write cycle or not. This feature is initiated by the stop condition after inputting write data. This requires the 8-bit device address word following the start condition during a internally-timed write cycle. Acknowledge polling will operate R/W code = "0". Acknowledgment "1" (no acknowledgment) shows the EEPROM is in a internally-timed write cycle and acknowledgment "0" shows that the internally-timed write cycle has completed. See Write Cycle Polling using ACK.

## Write Cycle Polling Using ACK



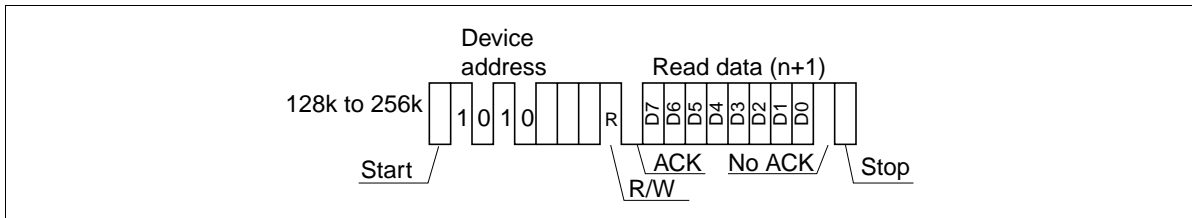
**Read Operation**

There are three read operations: current address read, random read, and sequential read. Read operations are initiated the same way as write operations with the exception of R/W = “1”.

**Current Address Read:**

The internal address counter maintains the last address accessed during the last read or write operation, with incremented by one. Current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word (R/W is “1”), the EEPROM outputs the 8-bit current address data from the most significant bit following acknowledgment “0” If the EEPROM receives acknowledgment “1” (no acknowledgment) and a following stop condition, the EEPROM stops the read operation and is turned to a standby state. In case the EEPROM have accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case the EEPROM have accessed the last address of the page at previous write operation, the current address will roll over within page addressing and returns to the first address in the same page. The current address is valid while power is on. The current address after power on will be indefinite. The random read operation described below is necessary to define the memory address.

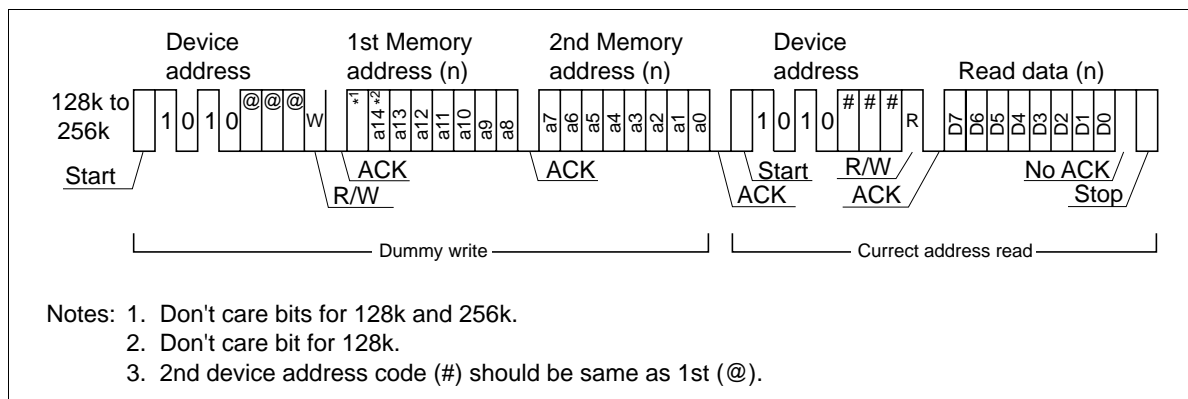
**Current Address Read Operation**



## Random Read:

This is a read operation with defined read address. A random read requires a dummy write to set read address. The EEPROM receives a start condition, device address word (R/W=0) and memory address  $2 \times 8$ -bit sequentially. The EEPROM outputs acknowledgment "0" after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving acknowledgment "1"(no acknowledgment) and a following stop condition, the EEPROM stops the random read operation and returns to a standby state.

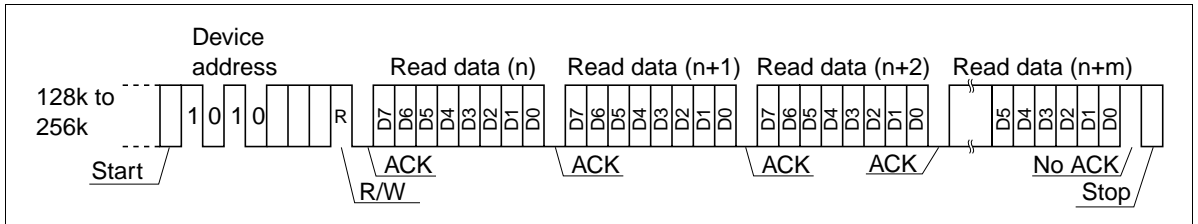
## Random Read Operation



**Sequential Read:**

Sequential reads are initiated by either a current address read or a random read. If the EEPROM receives acknowledgment “0” after 8-bit read data, the read address is incremented and the next 8-bit read data are coming out. This operation can be continued as long as the EEPROM receives acknowledgment “0”. The address will roll over and returns address zero if it reaches the last address of the last page. The sequential read can be continued after roll over. The sequential read is terminated if the EEPROM receives acknowledgment “1” (no acknowledgment) and a following stop condition.

**Sequential Read Operation**



## Notes

### Data Protection at $V_{CC}$ On/Off

When  $V_{CC}$  is turned on or off, noise on the SCL and SDA inputs generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to unintentional program mode. To prevent this unintentional programming, this EEPROM have a power on reset function. Be careful of the notices described below in order for the power on reset function to operate correctly.

- SCL and SDA should be fixed to  $V_{CC}$  or  $V_{SS}$  during  $V_{CC}$  on/off. Low to high or high to low transition during  $V_{CC}$  on/off may cause the trigger for the unintentional programming.
- $V_{CC}$  should be turned off after the EEPROM is placed in a standby state.
- $V_{CC}$  should be turned on from the ground level( $V_{SS}$ ) in order for the EEPROM not to enter the unintentional programming mode.
- $V_{CC}$  turn on speed should be longer than 10  $\mu$ s.

### Write/Erase Endurance and Data Retention Time

The endurance is  $10^5$  cycles in case of page programming and  $10^4$  cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than  $10^4$  cycles.

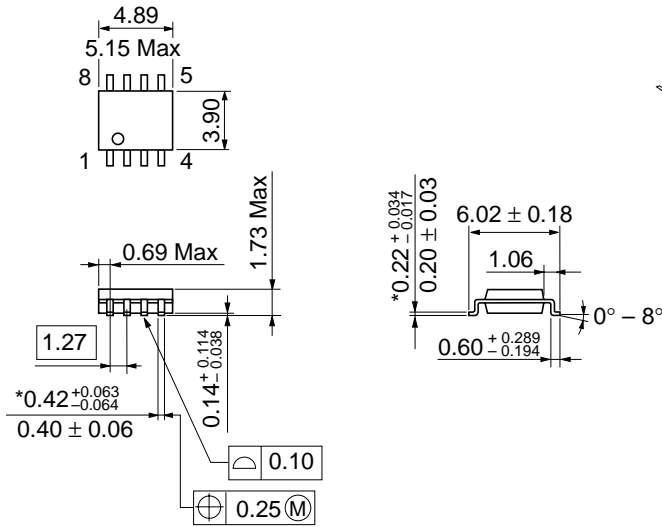
### Noise Suppression Time

This EEPROM have a noise suppression function at SCL and SDA inputs, that cut noise of width less than 50 ns. Be careful not to allow noise of width more than 50 ns.

## Package Dimensions

HN58X24128FPIAG/HN58X24256FPIAG (FP-8DB)

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-8DB
JEDEC	—
EIAJ	—
Mass (reference value)	0.08 g

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
             Europe                 : <http://www.hitachi-eu.com/hel/ecg>  
             Asia                         : <http://sicapac.hitachi-asia.com>  
             Japan                         : <http://www.hitachi.co.jp/Sicd/indx.htm>

## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.  
Electronic Components Group  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585200

Hitachi Europe GmbH  
Electronic Components Group  
Domacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00  
Singapore 049318  
Tel : <65>-538-6533/538-8577  
Fax : <65>-538-6933/538-3877  
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road  
Hung-Kuo Building  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
Fax : <886>-(2)-2718-8180  
Telex : 23222 HAS-TP  
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel : <852>-(2)-735-9218  
Fax : <852>-(2)-730-0281  
URL : <http://semiconductor.hitachi.com.hk>

Copyright © Hitachi, Ltd., 2001. All rights reserved. Printed in Japan.

Colophon 4.0